Assessing Reliability of Embedded Resistor Designs in Integrated Circuit

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Introduction

Finite element analysis (FEA) has been widely adopted in semiconductor integrated circuit (IC) industry for evaluating and optimizing design functionality and reliability in the technology development phase [1.2]. The most common applications in this field include the simulation of local mechanical stress, temperature and electrical current distributions within IC devices and structures under specified operating conditions. Such capability allows validation of device structure design with quick turnaround time before or during fabrication process development.

As an example, electromigration, or biased metal ion diffusion in interconnecting wires under electrical loading, is one of the major reliability concerns in IC [3,4,5]. Driven by temperature and electrical current, electromigration causes metal depletion at flux divergence site and eventually leads to voiding and open circuit failure. Estimating temperature and current for each wire under operating condition is thus critical during IC design to ensure product reliability. In this paper, we present an example of using FEA to study the electromigration reliability of on-chip embedded resistor designs for IC, and to make design modification to avoid possible electromigration degradation in final product. Modeled hypothetical resistor structures comprise a resistive element and contacting metal wires embedded within silicon dioxide dielectrics and silicon substrate. The simulated current distributions and the resulting Joule heating are then used to assess electromigration reliability for design improvement.

Theory

Black's equation is used to translate the modeled temperature and current values to resistor lifetime, or mean-time-to-failure (MTTF), as described as follows [6]

$$MTTF \propto j^{-n} \exp\left(\frac{Q}{k_B T}\right)$$

where j is the current density along lateral direction of the conducting wire, n is the current exponent, Q is the activation of electromigration process, k_B is Boltzmann's constant and T is the temperature in °K. Based on the equation, the relative *MTTF* among different interconnects in the resistor structure can be compared to identify the weak link.

Governing Equations

The current project focuses primarily on the examination of thermal distribution and hotspots within a three-dimensional solid domains of highly resistive resistor, electrically connected aluminum wires, and the embedding insulators made of silicon compound. The heat transfer between the resistors, metal lines, and the insulation materials will be mainly facilitated using thermal conduction assuming perfect contact between any two material surfaces. In the multi-physics model, the Electric Currents physics is coupled with the default Heat Transfer in Solids module via Electromagnetic Heating Multiphysics interface.

Focusing on the steady conduction problem, the governing equations involved in the analysis neglect the unsteady term and the radiation term;

$$\rho\, C_p\, (\boldsymbol{u} \cdot \nabla T) + \nabla \cdot \boldsymbol{q} = Q + Q_{ted}$$

Here, the first and second terms on the left hand side represent the convection term that controls any heat transferred via fluid flow and the heat conduction term. On the right hand side, the first Q term represents heat generation (or loss) occurring in the body while the second Q_{tad} accounts for thermoelastic effects in the solid, which is not included in current investigation.

Following Fourier's law of heat conduction, the heat flux $\boldsymbol{q}$ is proportional to the temperature gradient ∇T:

$$\boldsymbol{q} = -k\, \nabla T$$

And the Joule heating equation that governs the resistant heat

$$\nabla . \boldsymbol{J} = Q_{j,v}$$
$$\boldsymbol{J} = \sigma \boldsymbol{E} + \boldsymbol{J_e}$$
$$\boldsymbol{E} = -\nabla V$$

The coupling between the two physics is achieved by the incorporation of resistive heating (ohmic heating) due to the electric current into the heat generation $\boldsymbol{Q_e}$

$$\rho\, C_p\, (\boldsymbol{u}\ \cdot \nabla T) + \nabla \cdot \boldsymbol{q} = \boldsymbol{Q_e}$$
$$\boldsymbol{Q_e} = \boldsymbol{J} \cdot \boldsymbol{E}$$

Here, the $\boldsymbol{J}$ and $\boldsymbol{E}$ are the current density and electric field strength, respectively.

Model Description and Material Selection

The 2D diagram of two structures (A and B) of the embedded resistors and metal wires being studied are depicted in Figures 1 and 2 below. The width of this metal structure (into the paper) is 12 µm. On Structure A, the resistor is connected to three (3) parallel aluminum wires with different cross section areas. The wires are also interconnected using tungsten legs (short metals). The significant amount of heat and current transfer from the resistor are expected to be distributed among these wires. Nevertheless, we hypothesize that as Wire 01 carries high current density and temperature, and therefore it will be prone to failure due to the electromigration. This weakness will be assessed using Black's equation described above after the evaluation of temperature and current density distribution.

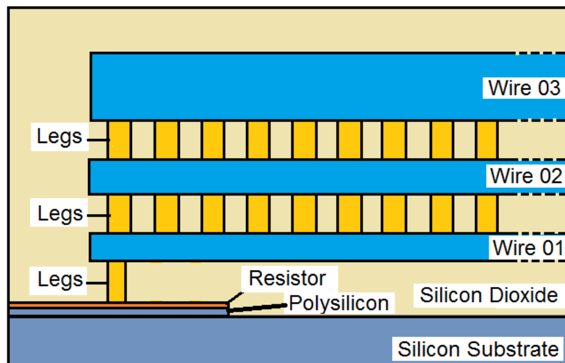

Figure 1. The diagram showing half of Structure A of the resistor architecture employed in the study. The thickness and material properties of the components are presented in Table 1.

Structure B presented in Figure 2 below utilizes only one wire to transfer the current and heat (Wire 03). The ends of Wires 01 and 02 are still included as shown in the diagram for electrical conduction. This metal is expected to transfer heat into the surrounding insulator and other metal wires, but they will not carry current in the major current direction (x- direction). Therefore, these metal wire ends are expected to be immune from electromigration.

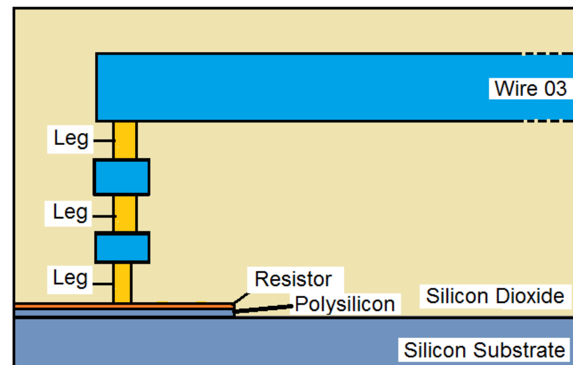

Figure 2. The diagram showing half of Structure B which lacks wires 01 and 02.

To carry out the study, material properties are selected for the conducting metals and the insulator. The hypothetical 0.1 µm-thick resistor is assumed to have k of 50 W/mK and σ = 3e6 S/m. Other parametric values may be selected for the resistors, however the current study focuses on the architectural consideration instead of effects of material selection.

Table 1. Thermal conductivity (k) and electrical conductivity (σ) of the materials used in the study. The resistor is assumed to have $k = 50\ W/mK$ and σ = 3e6 S/m

Materials	$\boldsymbol{k}$ ($\frac{\mathrm{W}}{\mathrm{mK}}$)	$\boldsymbol{\sigma}$ ($10^5 \frac{S}{m}$)	Purpose
Aluminum	235	350	Wires
Tungsten	175	179	Legs
Polysilicon	130	~0	Insulators
Silicon Dioxide	1.4	~0	Insulators
Silicon Substrate	130	~ 0	Insulators
Resistive Material	50	30	Resistor

A reasonable geometrical dimension selected for this study is tabulated in Table 2 below. Due to the lateral symmetry of the model (along the y direction – see Figure 3), only half of the embedded structure is presented here. Due to the applied potential difference in the x-direction (see Figure 3), the geometrical and thermal symmetry in this direction cannot be utilized. The length of the resistor is assumed to be 42 µm. And the length of the wires are selected to be 32.2 µm. The total length of the model is 100 µm. The width of the metal structure is only 6.0 µm. Nevertheless, the total width and depth of the silicon substrate are selected to be both 50 µm in order to make sure that the lateral boundary effects can be neglected.

Boundary Condition and Mesh Density

The boundary conditions (BC's) are described in Figure 3 below. The primary BC is the application of an electrical potential of 2.5 V on the wire ends (left ones). Also on this end, thermal BC temperature of 298.15 °K (room temperature) is applied. The other wire ends (right side) are assumed to electrically behave as "Ground" having the same temperature BC as the other end. The thermal symmetry BC is applied on the symmetry plane of the model. The bottom of the silicon substrate is assumed to have room temperature as well.

Table 2. The dimension of components used in the models.

Name	***h*** **(μ)**	***w*** **(μ)**	***L*** **(μ)**
Resistor	0.1	6.0	42.0
Wire 01	0.65	6.0	32.2
Wire 02	0.80	6.0	32.2
Wire 03	3.00	6.0	32.2
Single Leg	0.40	6.0	0.95
Top Leg	0.55	6.0	0.90

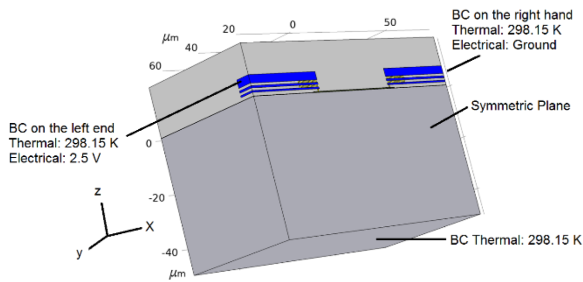

Figure 3. The boundary condition applied on the 3D geometrical model of metal interconnect and resistor (highlighted) embedded in silicon (insulator). The x-direction is taken along the long axis of the metal structure.

To carry out the simulation, the 3D model is discretized using mainly free tetrahedral elements. The "General Physics" option with "Predefined - Finer" mesh are selected. This mesh is the minimum mesh density that will not cause the "warnings" sign on the mesh quality to be displayed. The selected mesh density results in number of elements of 1499561 (about 1.5 million elements) and minimum element quality of 0.03602. The "extra fine" option would result in 11730877 number of elements, almost 10 times more than the "Finer" option. This mesh selection results in significant amount of processing time with minimum improvement on the results.

Simulation Results and Discussion

The 3D distribution of temperature rise (ΔT) shown in Figure 4 demonstrates the expected heating in the resistor obtained for Structure A. Noting that the temperature shown is relative to the BC's temperature of 298.15 °K, the warmest region in the resistor can reach about 200 ºC in temperature increase.

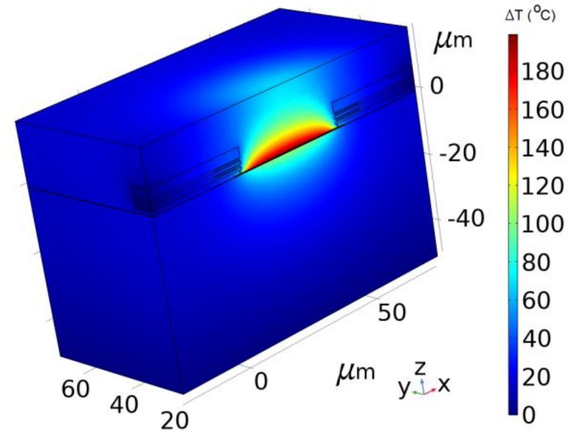

Figure 4. The 3D temperature distribution of Structure A above shows the concentration of maximum temperature on the resistor in its embedding insulation.

The 2D distribution of temperature rise on the resistor plane from Structure A (Figure 5) shows that the distribution is two-dimensional and symmetrical, as expected. The almost-zero region on both ends of the resistor is caused by the lack of current flow in that region. The high temperature area is located in between the two legs connecting the resistor to Wire 01.

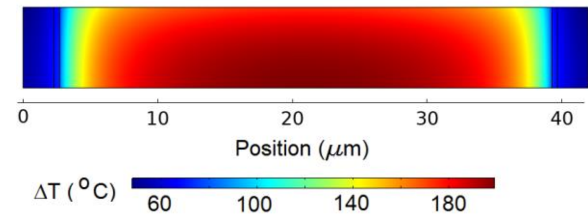

Figure 5. The temperature map on the top surface of the resistor showing two dimensional and symmetrical characteristic. The area with high temperature is located in between the legs A that connect the resistor to the Wire 01.

The temperature rises for both Structures A and B are plotted along a line parallel to the x-axis on the middle plane of the resistor (Figure 6). The plots indicate that the temperature distribution in the resistor is not affected by the removal of Wires 01 and 02. In fact, the modification results in a slight drop of temperature.

On the other hand, the plots of total current in the x-direction in the resistor of both Structures A and B (Figure 7) show identical results. The plots also indicate that the current can be considered to be constant along the resistor, as is expected. The effective length of the resistor with non-zero current

spans between the two legs connecting the resistor to Wire 01. The total current in the resistor can be verified after estimating the resistance R of the resistor using

$$R = \frac{1}{\sigma} \frac{L_e}{(w * h)} = 20.3\ \Omega$$

where L_e is the effective length on the resistor taken between the two legs that connect the resistor to Wire 01 on both ends. The total current can be estimated from the known relation to be

$$I = \frac{V}{R} = \frac{2.5}{20.3} = 0.123\ \text{A}$$

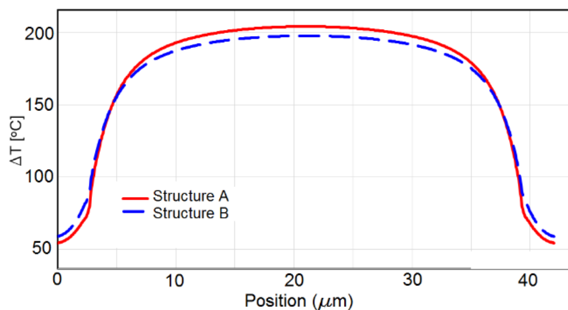

Figure 6. Temperature distributions along the cutting line set at the middle of the resistor for Structure A and B.

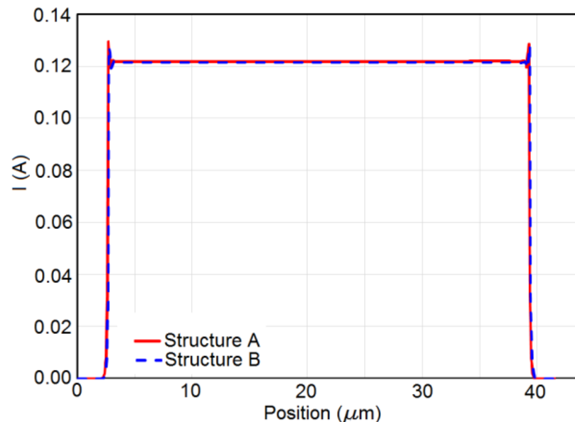

Figure 7. Distributions of total current in the x-direction along the resistor, which are identical for both Structures A and B. The zero current is associated with the region of the resistor beyond the contacting legs.

Along the wires, the temperature changes from the highest on the wire edge near the resistor to the BC temperature on the other wire end. For Structure A, the maximum temperature rise varies between 40 to 53 ºC. As expected, Wire 01 has the highest temperature because it is located nearest to the resistor. For Structure B, the maximum temperature on Wire 03 is less than 50ºC, lower than that of Structure A.

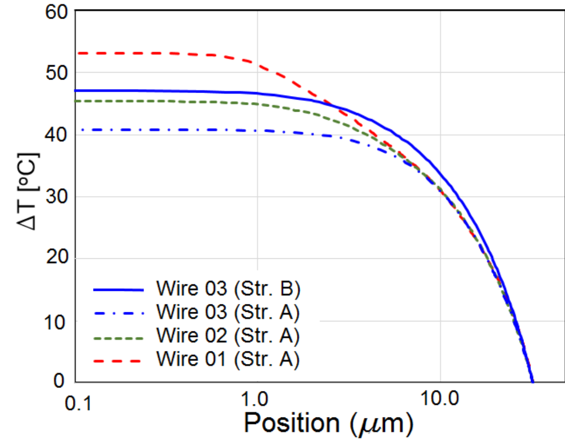

Figure 8. Temperature distributions along Wires 01, 02, and 03 for Structure A and Wire 03 for Structure B. Note that the zero position (left end) is located at the end of the wires connecting to the resistor (see Figures 1 and 2)

The simulated current density (*j*) along the x-direction are shown in Figure 9. The plots show significant increase in current density in Wire 01 due to the presence of tungsten legs that transfer the current from Wires 03 and 02 into Wire 01. The lack of smoothness on the current density of Wires 01 and 02 may be attributed to the insufficient mesh density for the wires, as well as to localized current flow along the y-direction in the region containing the contacting legs.

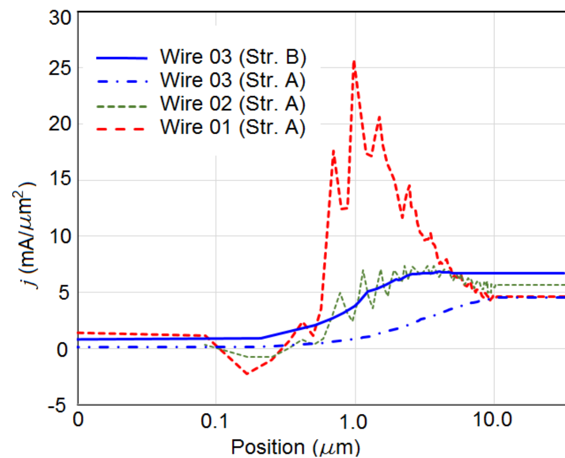

Figure 9. Plots of current density distribution along the wires for Structures A and B. The zero position is located at the end of the wires that are connected to the resistor via legs A.

Results of the above Joule heating modeling, i.e. local temperature and current density distributions as shown respectively in Figures 8 and 9, are used to assess electromigration reliability of resistor wires. Table 3 summarizes the maximum temperature T_{max} and current density j_{max} near the end of each wire in the structures where electromigration-induced voiding is expected to occur. The corresponding *MTTF* for each

wire, normalized by Wire 01 in Structure A, can then be determined using Black's Equation to compare the relative lifetimes [6].

Table 3. Maximum modeled temperature and current density near end of each wire, and the corresponding relative *MTTF*'s estimated from Black's Equation.

Structure	Wire	T_{max} (°C)	j_{max} (mA/μm^2)	Relative *MTTF*
A	01	78.1	18.2	1.00
	02	70.3	5.40	14.3
	03	65.8	1.22	259
B	03	72.1	5.42	12.4

For Structure A where the resistor element is connected by three stacked wires (Wires 01, 02 and 03) for carrying lateral current in parallel, Wire 01 has the lowest *MTTF* due to its highest local temperature and current density among the three wires. Note that electromigration failure in Wire 01 leads to open circuit failure in the entire resistor structure, thus the lifetime of Structure A is limited by that of Wire 01 with relative *MTTF* of 1.

On the other hand, although Structure B also comprises three stacked wire levels, the two lower wires (Wires 01 and 02) are shortened to only transport current vertically up to Wire 03. All the lateral current flow, which is responsible for electromigration degradation, is handled by Wire 03. Therefore, the lifetime of Structure B is dictated by that of Wire 03 with a relative *MTTF* of 12.4, significantly higher than Structure A. As a results, it is expected that Structure B is a better design between the two structures with enhanced reliability against electromigration.

Conclusions

An example of employing finite element modeling to assess the reliability of embedded resistor structures in IC chips is presented. Distribution of both temperature and current along each connecting metal wire are modeled for two resistor structures via Electromagnetic Heating Multiphysics, and the simulated values are then translated to electromigration lifetime of each wire through Black's equation. It is clear that finite element modeling offers valuable insight for IC manufactures to explore design space for functionality and reliability with minimal turnaround time and cost. Future work remains to experimentally demonstrate the simulation results by fabricating the resistor structures for reliability stress and failure investigation.

References

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