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SELF-HEATING EFFECT IN SILICON NANOWIRES FIELD-EFFECT TRANSISTORS

D. Caina[1]
1. Faculty of Science, Universidad Central del Ecuador, Quito, Pichincha, Ecuador.

Abstract
Since conventional silicon metal-oxide-semiconductor field-effect transistor (MOSFET) is approaching its scaling limit, novel devices structures are being explored lately. The scaling of the technology to dimensions below ~45 nm, where short channel effects start to become significant. Nanowire Field-Effect Transistors are being investigated to solve short-channel effects (SCE) in future MOSFET technology. Silicon Nanowire Field-Effect Transistor (SiNWT) has attracted broad attention among them. There are more and more devices per unit area results in increasingly large amounts of heat generated per unit volume. Self-heating may lead to a substantial increase in the effective operating temperature of the device, which degrades the device electrical performance and affects device reliability. The present project aims to localize the hot spot in the SiNWT, and to plot the distribution of the heat in the channel of it.

Keywords: Self-heating, SiNWT, MOSFET, Joule effect, COMSOL

Introduction
Since conventional silicon metal-oxide-semiconductor field-effect transistor (MOSFET) is approaching its scaling limit, novel devices structures are being explored lately. The scaling of the technology to dimensions below ~45 nm, where short channel effects start to become significant. Nanowire Field-Effect Transistors are being investigated to solve short-channel effects (SCE) in future MOSFET technology. Silicon Nanowire Field-Effect Transistor (SiNWT) has attracted broad attention among them [1].
On one hand, reducing the transistor active area lowers the power requirements, since the voltage needed for the device operation is reduced accordingly to its size. On the other hand, loss of electrostatic control, mobility degradation, SCE, and the inability to further reduce the series resistance are some of the main drawbacks arising from the device shrinking. Furthermore, reducing the MOSFET area impacts the reliability and variability of such devices [2].
There are more and more devices per unit area results in increasingly large amounts of heat generated per unit volume. Self-heating may lead to a substantial increase in the effective operating temperature of the device, which degrades the device electrical performance and affects device reliability. Related to this phenomenon, many studies show details of Joule heat generation in silicon, as well as the effects of self-heating on scaling options of ultra-thin transistors[3].
To understand the device physics in depth and to assess the performance of SiNWT, simulation is important. Computer-aided-design tools can reduce both the cost and the development time of these silicon nanotransistors. From the previous assessment, our study is based on simulation by using COMSOL multiphysics software.
The present project aims to localize the hot spot in the SiNWT, and to plot the distribution of the heat in the channel of the SiNWT, in order to better understand of self-heating on the device performance from an electrical standpoint is discussed. For this purpose, the simulation results will be compared with the reported results in the literature.

Theory
Silicon Nanowire Transistor
The SiNWT enable the ultimate complementary metal oxide semiconductor (CMOS) device scaling with the best possible short-channel control, considering the quantum confinement effects and the scattering at atomic dimensions. Gate-All-Around (GAA) SiNWT is among the most suitable, for this new CMOS technology due to its immunity against SCE. GAA-SiNWT have a smaller channel and large surface-to-volume ratio comparing to planar devices based on bulk materials. In addition, the gate-surrounding or GAA structure in the nanowire transistor allows excellent electrostatic gate control over the nanowire channel. The GAA horizontal SiNWT architecture exhibits high similarities to the Fin Field-effect transistor (FinFET), which is the predominant technology in the current 10 nm or even 7 nm process node. Thus, GAA nanowire transistors are very promising candidates in the sub-7 nm nodes to extend the scalability beyond the limits imposed by the FinFET technology with much less complexity compared to the alternative scaling approaches [4].

In the GAA-SiNWT considered for this project, the current from the source to the drain is turned on and off by the voltage applied to the gate. Since the gate in nanowires is surrounding the channel, it can control the electrostatics of the channel more efficiently than the conventional MOSFET. As the switching time decreases, the active area in the device is heated up and becomes a veritable issue affecting electrical properties and reliability. A schematic illustration for this device is given in Figure 1.

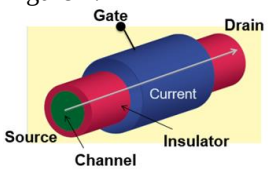


Figure 1. Geometrical structure of GAA-SiNWT.

Self-heating Effect

Self-heating effect (SHE) is a consequence of an accumulation of the heat in the channel, this accumulation is mainly at the drain side as depicted in Figure 2. SHE in silicon devices arises because of device scaling and the use of materials with low thermal conductivity such as SiO_2. Since the thermal conductivity is small, the thermal resistivity will be higher, and the heat will be more difficult to remove. This effect is detrimental for device performance and reliability, affecting the electrical properties of the transistor such as the threshold voltage, mobility and so on.

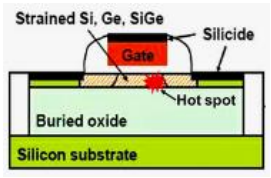


Figure 2. Location of the hot spot in SOI devices.

As mentioned, SHE can affect also GAA-SiNWT behavior by changing some electrical properties due to temperature dependent parameters such as carrier mobility (μ), threshold voltage (V_{TH}), velocity saturation (V_{sat}) and subthreshold slope (SS). The mathematical expressions are depicted in equation 1 to equation 4 [11].

$$\mu = \mu_0 (T_{eff}/T_0)^{\alpha} \quad (1)$$

$$V_T = V_{T0}\eta(T - T_0) \quad (2)$$

$$v_{sat} = \frac{v_{sat0}}{(1-\beta) + \beta.(T_{eff}/T_0)} \quad (3)$$

$$SS = SS_0.\frac{T_{eff}}{T_0} \quad (4)$$

Joule Heating

SHE in MOSFET devices are closely related to the Joule-heat generated in the channel. The basic approach to estimate the power dissipation in an electronic "classical device", is to express it with the equation 5 [3].

$$P = I^2(R - R_c) \quad (5)$$

The Drift-Diffusion approach for energy dissipation in transistors is used to compute the spatial distribution of power dissipation in a SiNWT, as given in equation 6; where the term **J.E** represents the Joule heating.

$$P''' = \mathbf{J}.\mathbf{E} + (R - G)(E_g + 3\kappa_B T) \quad (6)$$

Where:

J: current density

E: electric field

(R-G): recombination minus generation

E_g: band gap

T: lattice temperature

The result of the equation 6 can be implemented with a finite element method (FEM) software tool like COMSOL multiphysics.

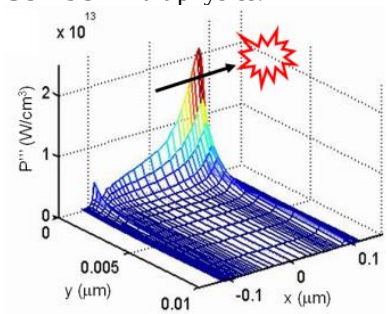


Figure 3: Drift-diffusion simulation of heat generation in MOSFET using equation 6 [3].

Simulation

COMSOL is a software based on Finite Element Method, which allows us to simulate self-heating using the Joule heating approximation. It was used with its Semiconductor module. Some previous studies have already used COMSOL to study the Joule heat and predict the localized temperature of the SiNWT [22].

COMSOL multiphysics uses the standard semiconductors equations 7 to 9. Nowadays there are many efforts to achieve new models and equations to simulate most accurate self-heating effects in such transistors. For instance, Hossain et al. (2010) use of the optical phonon and acoustic phonon energy balanced equations derived from the phonon Boltzmann equations, to investigate the role of self-heating effects on SiNWT using a 3-D Monte Carlo method [23].

$$\rho += q(p - n + N_d^+ - N_a^-) \quad (7)$$

$$J_n = qn\mu_n \nabla E_c + \mu_n K_B T \nabla n + qnD_{n,th}\nabla \ln(T) \quad (8)$$

$$J_p = qp\mu_p \nabla E_v - \mu_p K_B T \nabla p - qpD_{p,th}\nabla \ln(T) \quad (9)$$

with $\nabla.J_n = 0, \nabla.J_p = 0$, $E_c = -(V + \chi_0)$, $E_v = -(V + \chi_0 + E_{g,0})$

Some studies combined techniques to carry out simulations. For example, [7] combined DD and MC techniques. In the same way, the DD model is preferred for the simulation of subthreshold region due to time efficiency and because the particle-based MC method can be noisy at very small currents, and DD consumes less time than MC technique.

Domain of Simulation

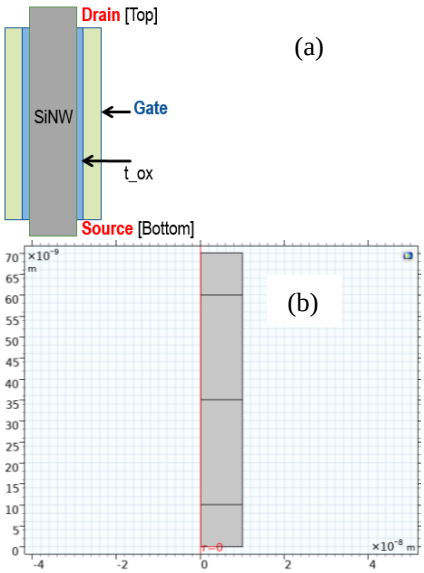
The dimensions in Table 1 were considered for this project, in order to simulate the SHE in SiNWT. Those values are common for SiNWT and they allowed to determine the convergence of the solver in COMSOL simulator.

The schematic illustration and geometry of the SiNWT being simulated in this project is illustrated in Figure 4(a)(b). We used an axisymmetric geometry for defining the parameters in COMSOL, but the simulation results are computed for 3D dimensions. The gate, source and drain contacts are considered like electrodes, according to the available boundary conditions in COMSOL.

The source and drain contacts are boundaries that are treated as ideal ohmic contacts. SiNWT has a relatively low-doped channel region and heavily doped S/D region, as depicted in Figure 4(c) with the profile of the doping. The Nanowire is isolated from the metal gate with a thin layer of SiO_2 of 2 nm.

Name	Expression	Description
Rw	10[nm]	Radius Nanowire
t_ox	2[nm]	Oxide thickness
L	50[nm]	Channel length
T0	300[K]	Room Temperature
Na_0	1e17[1/cm^3]	Acceptors
Nd_0	1e20[1/cm^3]	Donors
ε_{ins}	3.9	Oxide relative permittivity
Φ	4.3 [V]	Metal work function

Table 1: Parameters for simulated SiNWT in COMSOL.



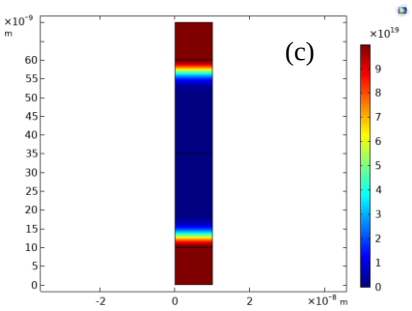


Figure 4. (a) Schematic of SiNWT, (b) Geometry of SINWT and (c) doping level in COMSOL.

In the simulations presented in this report, we consider the room temperature. If different boundary conditions of temperature are needed, the heat transfer module of COMSOL must be used, in order to set up different boundary conditions for the temperature.

Simulation Results

This section presents the results of simulation using COMSOL. Here, we show elements from I-V curves of SiNWT and its temperature distribution in the channel.

The current-voltage characteristics obtained by simulation (bottom panel) are similar to those obtained by Colinge et al. (2010) [24] (top panel), which show that the device behaves like a transistor.

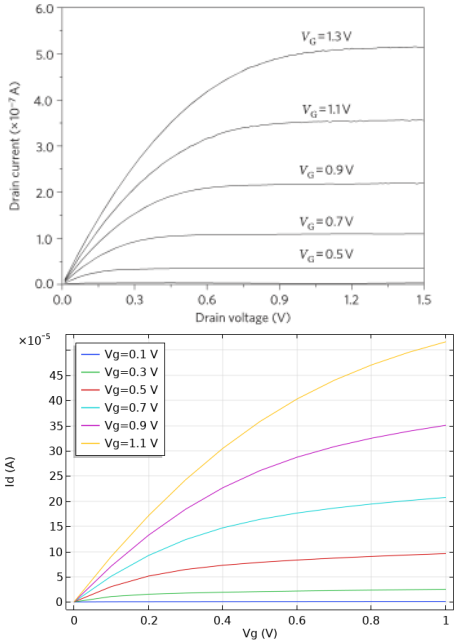


Figure 5. (Top) I–V curve for n-type transistor [24], (bottom) I-V curves obtained by simulation.

Simulation Joule Effect

As we mentioned in the early sections, the hottest spot on the self-heated SiNWT by Joule heating appears close to drain side.

According to [18], the electro-thermal modeling is based on an assumption that thermal resistance of the device is independent of the applied voltage. With this assumption, the temperature rise at hotspot

should be linearly increases as the input power increases, as depicted in equation 11.

$$\Delta T_{SHE} = P''' * R_{TH} = I_D * V_D * R_{TH} \quad (11)$$

Where,

P'''= the amount of power being dissipated.

ΔT= the expected temperature change at hot spot.

R_{TH}= the total thermal resistance in the heat flow path.

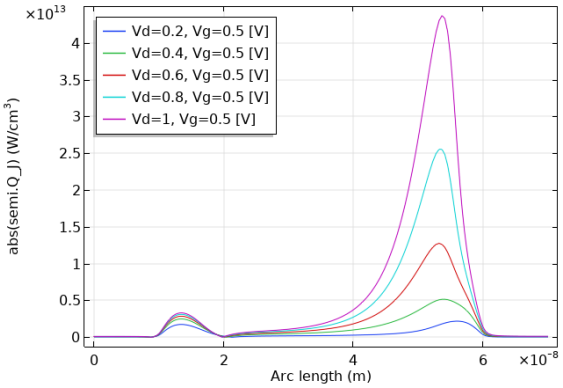


Figure 1. Distribution of the heat in the SiNWT channel.

The values of R_{TH} was taken from other experimental studies, where the AC conductance technique was adopted to extract R_{TH} [6] [20]. This technique also is adopted to characterize SHE as we explained in previous section.

Nanowires with radius of 8 nm, 10 nm, 12 nm were simulated using COMSOL with all other dimensions constant as listed in Table 1. Nanowire with 8 nm radius presents more gradient of temperature in the channel than the one with 12 nm radius. Figure 7 shows the extracted average channel temperature in SiNWT as a function of power.

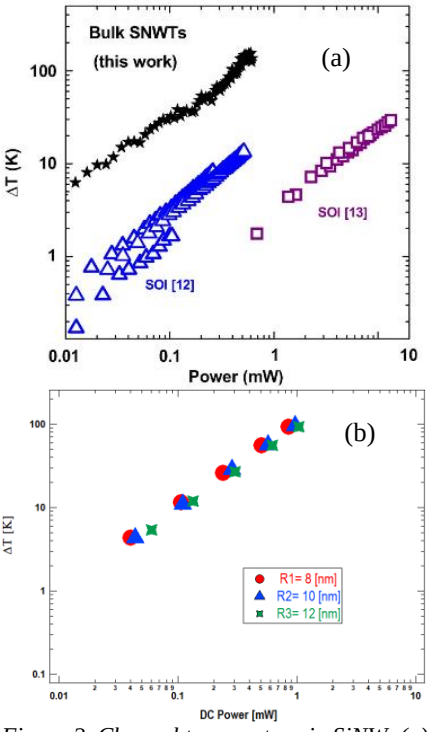


Figure 2. Channel temperature in SiNW (a) reported by Wang et al. [6], and (b) results from COMSOL simulations.

It can be observed that the ΔT from the Figure 7(a) is comparable to that of simulations results in Figure 7(b), where for a DC power of 1 mW we have around an ΔT of 100 K. Comparing with other MOSFET devices, SiNWT shows stronger self-heating than SOI devices and tend to be heated more quickly. It can also be seen from Figure 7(b) that the slope of the line represents the R_{TH}, and it increases when the diameter decreases.

Discussion

In this section, we discuss some important aspects of the simulation results, and we indicate future research directions related to this tremendous topic.

For instance, heat transport is a critical issue to consider for determining SHE in GAA-SiNWT due to the low thermal conductivity. As example in [23], the SHE is more pronounced in SiNWTs with similar channel length as the FD SOI devices due to the worse heat transport.

We consider for our project that thermal resistance is independent of the applied voltage according the assumption by Wang et al. (2008) [18]. From this point of view, our obtained results are similar to the ones reported in [6].

COMSOL simulation can be enhanced and combined with other physical phenomenon, in order to evaluate most accurate the SiNWT and its SHE. For instance, the heat transfer module can be used for defining different boundary and internal conditions, for applying a wide range of temperature and not only room temperature as considered in this project. Structural mechanics module is also of interest in COMSOL, which can be used for studying the effects of the strain in SiNWT. Both modules must be combined with the Semiconductor module.

We have investigated that it is possible to do the gate and contacts in 3D by COMSOL, however, additional features of the simulator are needed master beyond Semiconductor module, like convergence models, combining of meshing types and so on.

Nowadays experimental results can be associated to simulations results as we demonstrate in this project. Also theoretical models can be used to validate experimental results like Huang et al. (2012) demonstrate with an electro-thermal model for GAA SiNWT which takes into account critical issues like the geometry and the roughness [11].

Conclusions

In summary, in this project we have presented preliminary simulation results for SHE in SiNWT. The location of the hot spot in the GAA-SiNWT was determined and showed by plotting the distribution of the heat in the channel with respect to the geometrical parameters of the SiNWT. For instance, the results show that the diameter of SiNWTs is an

important factor that influence the self-heating effect. The 8 nm radius has more heat in the channel than the one with 12 nm.
In this project, the self-heating effect using Joule heating has been determined in GAA-SiNWT. The results indicate that they are in concordance with the reported results in the literature. The SHE in SiNWT is more pronounced than that in SOI devices due to the 1D nature of nanowire and increased phono-boundary scattering within it.
In this project, the obtained results for I-V curves were obtained qualitatively and quantitatively and they are similar to the reported results from the literature.
We can point out that the self-heating effect in SiNWT is due to the low thermal conductivity of the silicon at nanoscale, thus, the heat inside the channel that cannot dissipate easily.
The accuracy of results obtained in this project can be improved considering other issues, such as the geometry and surface roughness of NWs, doping concentration, length of the channel, as well as, different materials like SiGe and so on. All these aspects can be addressed to derive even more conclusive results regarding self-heating in SiNWTs.

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